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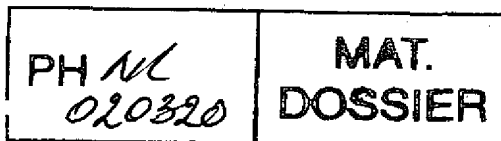
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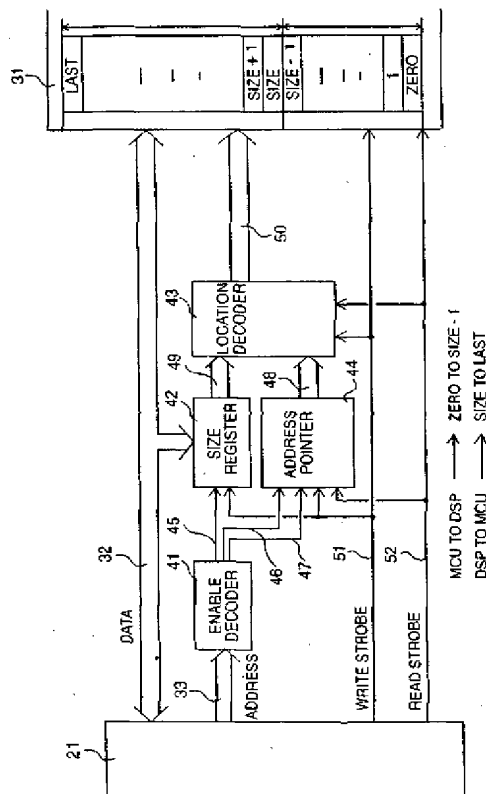
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(54) Data interface

(57) A data buffer (23) is positionable between processing devices, such as microcontroller (21) and a digital signal processor (22). Messages are transmitted between the devices via a dual port RAM buffer (31). The amount of storage allocated for transfers in each

direction is adjustable via a size register (42) so that, at any particular time, the optimum amount of storage is provided for a transfer in a particular direction. The buffer is particular suited to applications in mobile telephones.

**Figure 4****EP 0 729 106 A1**

Description

The present invention relates to a data interface positionable between a first processing means and second processing means.

A trend in recent years has been towards distributed systems, in which a plurality of independently programmable processing devices are mutually connected. An advantage of using interconnected but independently controllable devices is that the devices may function under differing operating conditions. For example, multi-purpose microprocessors and microcontrollers are capable of performing a large range of activities, particularly in a control environment. However, when processing digitised signals in real-time, a higher rate of processing is often required and this may be achieved using devices constructed for performing a relatively low number of high speed real-time operations, including signal multiplications. Devices of this type have become known as digital signal processors and these processors may be acquired as general purpose devices or included as part of an application specific integrated circuit.

A problem with including different types of processing devices within a common working environment is that difficulties occur when it is necessary for the processors to communicate. A particular problem occurs when microcontrollers are required to communicate with digital signal processors, given that digital signal processors generally operate at a much higher speed than microcontrollers and the rate at which data is generated by a digital signal processor may be far greater than that at which a microcontroller may be able to accept it. Similarly, if the digital signal processor is instructed to receive data from a microcontroller, it may be frozen out from doing other work for a relatively long period of time, thereby reducing the overall efficiency of the system.

According to an aspect of the present invention, there is provided a data interface positionable between a first processing means and a second processing means, comprising storage means arranged to buffer data signals generated by each of said processing means, and storage allocation means arranged to adjust the amount of said storage available for transfer in each particular direction.

Thus, an advantage of the present invention is that it provides a continually addressable storage area which may be addressed so as to buffer data generated by the first processing means, for transfer to the second processing means, or to buffer data generated by the second processing means for transfer to the first processing means. At any one time, a particular storage location is allocated for transfer in one of said directions. However, the storage allocation means is provided to adjust the allocation, such that maximum benefit is derived from the available memory locations.

In a preferred embodiment, the adjustment of mem-

ory allocation is made in response to requests by one or both of said processing means.

Preferably, one of said processing means is a digital signal processor. Preferably, one of said processing means is a microcontroller or a microprocessor.

In a preferred embodiment, the interface is positionable between processing means provided within a mobile telephone.

The invention will now be described by way of example only, with reference to the accompanying drawings, in which

Figure 1 shows a mobile telephone with internal circuitry including a microcontroller subsystem and a digital signal processor subsystem;

Figure 2 illustrates the arrangement of the microcontroller subsystem and the digital signal processor subsystem of the telephone illustrated in Figure 1, including an data buffering for allowing communication between the subsystems;

Figure 3 details the data buffering circuit shown in Figure 2, including a dual port randomly accessible memory device and interface circuits connecting said memory device to a micro controller unit and a digital signal processor; and

Figure 4 details one of the interface circuits shown in Figure 3.

A mobile telephone is shown in Figure 1, having a mouthpiece microphone 15 and an earpiece loudspeaker 16. Conventional signalling buttons 17 are provided, enabling telephone numbers to be dialled and supplementary telephony services to be effected. A liquid crystal display 18 provides a visual display to an operator, arranged to display selected telephone numbers and provide indications of other operating characteristics.

The internal circuitry for the telephone shown in Figure 1 is shown diagrammatically in Figure 2, with similar references being given to similar components. The keypad 17 and the display 18 operate under the control of a microcontroller subsystem (MCU) 21. The microcontroller subsystem 21 is responsible for the overall operation of the telephone handset and is particularly important when overseeing signalling operations and controlling operating characteristics, such as effecting frequency modifications when operation is switched between cells. However, the microcontroller subsystem is not capable of processing real-time digital speech signals and for this purpose a digital signal processor subsystem (DSP) 22 is provided. Thus, the digital signal processor subsystem receives audio signals from the microphone 15 and supplies audio signals to the loudspeaker 16.

Although each processor performs its own specific tasks, it is necessary, at regular intervals, for the microcontroller subsystem 21 to communicate with the digital

signal processor subsystem 22. This communication is facilitated by the provision of a data buffering circuit 23. In particular, the microcontroller subsystem may write data to the buffer 23 which is internally buffered by said buffer, thereby allowing the microcontroller subsystem to resume its local processing. Once written to the buffer 23, data may be accessed by the digital signal processor subsystem 22, such that the transfer of data from the microcontroller subsystem 21 is effected under the control of its own system clock, at speeds compatible with the operation of the microcontroller subsystem 21, whereas the reception of data from the interface by the digital signal processor subsystem, is effected by its own internal clock, thereby ensuring that data transfer takes place at speeds compatible with the operation of both subsystems.

Similarly, data transfers may take place in the opposite direction. Thus, the digital signal processor subsystem 21 may write data to the interface 23, at rates compatible with the operation of said processor, whereafter the data may be read from the interface 23 under the control of the microcontroller subsystem 21.

The MCU sub-system 21 and the DSP sub-system 22 run programs which retain information identifying storage areas within the buffer area 23 to which each sub-system may write to and from which each sub-system may read from. After a sub-system has written data to the data buffer 23 it issues an interrupt to the other sub-system via an interrupt circuit 24. Thus, once interrupted via circuit 24, a sub-system will, when appropriate, execute a sub-routine so as to read the data from the data buffer 23 that has been written to said buffer from the other sub-system. The interrupt circuit 24 is also arranged to receive interrupt signals from other devices, not shown in Figure 2, prioritise these interrupts and, where necessary, mask interrupts to prevent essential operations from being disturbed.

The data buffer 23 is detailed in Figure 3. The buffer includes a dual port random access memory device 31 that may be provided, for example, with sixty-four addressable locations, each capable of storing 8 bits of data. Memory locations within the RAM 31 may be used to buffer data being transferred from the MCU system 21 to the DSP system 22 and to facilitate the transfer of data in the reverse direction, from the DSP sub-system 22 to the MCU sub-system 21. Thus, the buffer is effectively positionable between a first processing environment and a second processing environment and comprises storage arranged to buffer signals generated by each of the said processing environments. At any particular time, storage locations within the RAM 31 are allocated as being part of the storage available for transfers in one direction or for transfer in the other direction. Thus, interface circuits are provided that include registers for maintaining a record of the allocation of storage within the RAM 31 along with systems for effecting re-allocation so as to adjust the amount of storage available for transfer in each of the directions.

The MCU sub-system 21 has an associated data bus 32 and an associated address bus 33. Similarly, the DSP sub-system 22 has a data bus 34 and an address bus 35. The MCU data bus 32 is connected directly to the RAM 31, via its first port and, similarly, the data bus 34 of the DSP 22 is connected directly to the second port of the RAM 31.

The MCU address bus 33 is connected to an MCU interface circuit 36, which is also connected to the MCU data bus 32. Similarly, a DSP interface 37 receives address signals over the DSP address bus 35 in addition to receiving data signals from the DSP data bus 34. The MCU interface 36 and the DSP interface 37 provide addressing signals to the RAM 31 over respective RAM address lines 38 and 39.

Both the MCU sub-system 21 and the DSP sub-system 22 address storage locations within the RAM 31 as if they occupied a single addressable location. Thus, the respective address, representing the RAM 31, is supplied to address lines 33 or 35 which are in turn interpreted by the respective interfaces 36 and 37. When addressed in this way, a plurality of data words may be supplied to the respective data buses, 32 or 34, resulting in the data being written to the RAM 31 in response to address signals generated by the respective interfaces 36 and 37. Thus, the interfaces 36 and 37 include address pointers which are incremented as data is written to the dual port RAM 31. Similarly, these pointers are also incremented as data is read from the RAM 31.

A proportion of the storage locations within the RAM 31 are provided to facilitate transfers from the MCU 31 to the DSP while the remainder are provided to effect transfers in the opposite direction. However, the point at which the crossover occurs is adjustable and controlled in response to programs executed on the sub-systems.

In the preferred embodiment, only the MCU sub-system 21 is capable of adjusting the position at which the crossover occurs and when the DSP 22 requires additional storage locations within the RAM 31, it must request the MCU 21 to provide this additional space. Requests of this type are made by the DSP issuing a command which is supplied over address bus 34, stored within the RAM 31 and thereafter read from said RAM 31 and processed by the MCU 21. Thus, messages generated by the DSP 22 are encoded such that they will be acted upon by the MCU 21 or supplied to other processing equipment.

The MCU sub-system 21 includes a read-only flash memory. This memory is provided so as to retain programs executable within the MCU environment 21, along with programs executable within the DSP environment 22. Thus, the DSP is arranged to operate under instructions supplied from local volatile memory but, in response to a power-up condition, programs executable by the DSP sub-system 22 must be downloaded from the flash memory under the control of the MCU sub-system 21.

All transfers from the MCU sub-system 21 to the

DSP sub-system 22 are effected via the RAM 31, therefore, in order to effect the downloading of programs to the DSP sub-system 22, the split point of the RAM 31 is modified, such that the amount of buffering storage available for transfers from the MCU 21 to the DSP 22 is maximised. Thus, for example, in the embodiment where a total of sixty-four storage locations are provided, sixty-two of these locations may be allocated for transfers from the MCU 21 to the DSP 22, until the DSP has received a full complement of executable programs from the MCU's flash memory. Thereafter, the DSP may issue commands to the MCU so as to re-allocate the split point such that messages larger than 2 bytes may be transferred from the DSP to the MCU 21. In this way, the available capacity within the RAM 31 is optimised and allocated for transfers in either direction, substantially in response to instantaneous demand.

The MCU interface 36 is detailed in Figure 4 and includes an enable decoder 41, a size register 42, a location decoder 43 and an address pointer 44. The enable decoder 41 receives address signals from the MCU's address bus 33 and includes combinational logic arranged to detect specific address signals generated by the MCU. In particular, the MCU sub-system 21 may generate three specific addresses which are decoded by the enable decoder 41.

A first address signal, to which the enable decoder 41 is responsive, is interpreted by the enable decoder 41 resulting in an enabling signal being supplied to the size register 42 over an enabling line 45. Once enabled in this way, the variable "SIZE", stored in register 42, may be updated, in response to data supplied over the data bus 32. Thus, in this way, it is possible for the MCU sub-system 21 to effectively re-establish a new split point within the RAM 31.

The second address, to which the enable decoder 41 is responsive, is interpreted as an address pointer re-set signal which is supplied to the address pointer over a re-set line 46. In response to receiving a re-set signal, the address pointer 44 is re-set, so as to effectively re-initiate a reading or writing operation.

The third address, to which the enable decoder 41 is responsive, is interpreted as an address pointer enable command, resulting in an enabling signal being supplied to the address pointer 44 over an enabling line 47. Thus, when enabled in this way, the address pointer 44 generates incremental address signals, which are supplied to the location decoder 43 over a first internal address bus 48. A similar second internal address bus 49 supplies addressing signals from the size register 42 to the location decoder 43 and in response to these two signals an address signal is supplied to the RAM 31 over a third internal address bus 50.

Memory locations within the RAM 31 are schematically illustrated in Figure 4. Thus, the first addressable location may be identified as location "ZERO" and the last location may be similarly identified as location "LAST". In a preferred embodiment the RAM 31 con-

tains a total of sixty-four memory locations, from ZERO to sixty-three, i.e. last equals sixty-three. Each location is arranged to store an eight bit byte and at least two bytes must be reserved for transfers in each direction. It is essential for a reservation of this type to be made, such that bandwidth is provided, by means of these two byte locations, enabling requests for additional buffering space to be made from one environment to the other. In particular, given that the MCU sub-system controls the position of the split point, at least two bytes of data must be permanently allocated for transfers from the DSP to the MCU.

At any particular time, the position of the split point is known to both the MCU software, the DSP software and register 42. The register 42 is readable by both the MCU and the DSP 22 but it may only be written to by the MCU.

The value stored in the size register 42 defines the lowest location for transfers from the DSP to the MCU. The variable "SIZE" may therefore have a value anywhere between two, identifying location two within the memory and sixty-two, identifying location sixty-two in the memory, where location sixty-three is the last location in the said memory. Thus, transfers from the MCU to the DSP are made via locations ZERO to SIZE-1 and transfers from the DSP to the MCU are made by locations SIZE to LAST.

A location decoder 43 converts an address generated by the address pointer 48 into an address which may be used to address the RAM 31. The MCU software and the DSP software both know the availability of memory allocated for transfers in each direction, however the value of variable "SIZE" is also transferred to the location decoder 43, over bus 49, so as to provide a further mechanism, within the location decoder 43, to prevent the address pointer 48 straying beyond its allocated region during a read or a write operation. Furthermore, the location decoder 43 is also instructed, via appropriate read and write strobe signals, as to whether a write operation or a read operation is being executed. In this way, the addresses generated by the address pointer 44 may be used for both reading and writing, with an appropriate off-set applied by the location decoder 43 when reading.

As previously stated, when the system is initially powered up it is necessary for DSP programs to be transferred from flash memory, forming part of the MCU sub-system, to volatile memory associated with the DSP sub-system. Before such a transfer takes place, the value of variable "SIZE" is maximised (set to sixty-one in the preferred embodiment) so as to allocate as much memory as possible within the RAM 31 for transfers from the MCU to the DSP. Once the DSP software has been loaded, it is executed by the DSP and the overall system is brought into a fully operational state.

For the purposes of this disclosure, it is assumed that, for whatever reason, the DSP now requires to transfer data back to the MCU during a period when

transfers in the reverse direction are minimal. Thus, in order to optimise the rate of transfer from the DSP to the MCU, it is appropriate to allocate additional storage within the RAM 31 for transfers from the DSP to the MCU.

After the transfer of program data from the MCU to the DSP, the value of variable SIZE has been set to sixty-two, such that storage locations sixty-two and sixty-three are the only locations within memory 31 which are available for transfers from the DSP to the MCU. Consequently, the DSP writes a message to these locations requesting the MCU to adjust the size position.

At any point in time, the MCU 21 may write data via its data bus 32 or, to the exclusion of a write operation, it may read data over its data bus 32. Data transfers from the MCU, as part of a write operation, are effected by placing data lines of the data bus to the appropriate logical values representing the data to be transferred. Similarly, address lines on the address bus 33 are modified so as to represent the write address. These operations take a finite period of time, in order for data levels to reach their appropriate point. Thereafter, a write strobe signal, in the form of a rising edge, is applied to a write strobe line 51, resulting in the data defined by the data bus being written to the address specified by the address bus.

A similar operation is performed as part of the reading function. The data port of the MCU is placed in a condition whereby it is ready to receive data. Address lines on the address bus 33 identify the location from which the data is to be read. Thereafter, a read strobe, in the form of a rising edge, is generated on the read strobe line 52, resulting in the data identified by the address bus 33 being read to the MCU 21 over its data bus 32.

In the example identified above, the DSP sub-system will have written an instruction to locations sixty-two and sixty-three of the RAM 31 which will in turn instruct the MCU 21 to allocate more memory space within RAM 31 for transfers from the DSP to the MCU, i.e. to reduce the value of variable "SIZE".

After successfully writing the instruction to the RAM 31, the DSP sub-system issues an interrupt to the MCU via the interrupt circuitry 24 effectively instructing the MCU to the effect that it has been mailed a message which it needs to read from what may be considered as its mailbox.

The MCU responds to the interrupt by generating an address on its address bus 33 to the enable decoder 41 which is interpreted by the decoder as an address of the second type. Thus, in response to receiving this address signal, the enable decoder 41 generates a re-set signal for line 46, resulting in the address pointer being re-set to zero. Thereafter, an address of a third type is supplied to the enable decoder 41 resulting in the decoder supplying an enabling signal to the address pointer 44 over the enabling line 47. Thus, in response to this enabling signal, the address pointer 44 is effectively in-

structed to generate address signals to the location decoder 43.

The enabling address on address line 33 is maintained throughout the read operation, such that, from the MCU's point of view, a plurality of data bits are being received over its data bus in response to an address signal effectively addressing the same logical memory location. However, actual addresses to the dual port RAM 31 are incremented in response to address signals generated by the address pointer 44.

In response to address signals generated over address bus 33, data is read by the MCU over data bus 32 under the control of read strobe signals generated over the read strobe line 52. The read strobe signals are supplied to the address pointer 44 and are also supplied to the location decoder 43. In response to receiving a read strobe signal, the location decoder 43 is instructed to the effect that a transfer is taking place from the DSP to the MCU. Consequently, the area of storage within the RAM 31 which is to be addressed lies within the range defined by the variable SIZE to position LAST. Thus, under the present conditions, the location decoder 43 will only generate addresses over address bus 50 identifying location sixty-two and location sixty-three.

The address pointer 44 has been re-set therefore it will initiate the generation of address signals starting from address ZERO. On receiving the next read strobe on read strobe line 52, address pointer 44 generates a value over address bus 48 representing location ZERO within the RAM 31. However, given that the read strobe has also been supplied to the location decoder 43, an offset, equivalent to the value SIZE, specified by the value received from bus 49, is added to the address received from bus 48, resulting in address SIZE plus ZERO being supplied to bus 50 resulting in location sixty-two being addressed by said bus.

The read strobe on line 52 is supplied to the RAM 31, thus, as address SIZE plus ZERO is supplied over bus 50, the appropriate location is read within the RAM 31, resulting in the data stored at location SIZE plus ZERO, i.e. location sixty-two, being supplied to the MCU sub-system over data bus 32.

On the next cycle, the read address is maintained on bus 33 and the address pointer is maintained enabled. The address pointer is incremented and an address identifying location 1 is supplied on address bus 48. Again, this is offset by the value stored in the size register 42, resulting in the last location being read from the RAM 31 and the data stored therein being supplied to the MCU over data bus 32.

The data received over the data bus 32 will be interpreted by the MCU 21 and in this particular example, it will be interpreted to the effect that the DSP requires additional buffering capacity. In accordance with protocols established within the MCU software, a decision will be made as to the extent to which the value stored within the size register 42 should be increased.

An address signal of the first type is supplied to the

address bus 33, resulting in the enable decoder 41 generating an enabling signal over line 45 to the size register 22. The new value for the size register is supplied to the data bus 32 and this value is clocked to the size register 42 in response to a write strobe generated on line 51. The MCU 21 may now generate a message to the DSP to the effect that it has been given additional space within the RAM 31.

During normal operation, the MCU 21 may supply other information to the DSP sub-system 31, in addition to the downloading of its executable programs. The system will be arranged such that, under normal operation, the allocation of space within the RAM 31 will be more or less halved and additional allocation, for transfers in one direction or the other, will only be given if necessary.

To transfer data from the MCU to the RAM 31 an address of the second type is supplied to the enable decoder 41, resulting in the address pointer 44 being reset to zero. The MCU 21 then, as far as it is concerned, addresses a single logical location, representing the RAM buffer, by generating an address over bus 33 of the third type, resulting in the enable decoder 41 enabling the address pointer 44. The first data byte to be transferred is supplied to the data bus 32 and address pointer 44 generates its first address for address bus 48. The first address supplied from the address pointer to the location decoder 43 will be zero, given that the address pointer has been reset and, given that storage location ZERO to SIZE-1 are used for transfers from the MCU to the DSP, no offset will be added by the location decoder 43. However, the location decoder 43 will ensure that addresses generated by the address pointer 44 will not exceed address values supplied by the size register over bus 49.

A write strobe signal is generated over line 51, resulting in the data values supplied to the data bus 32 being written to location ZERO within the RAM 31. Once this transfer has been performed, the address pointer is incremented such that, on receiving the next write strobe signal on line 51, the next data value on bus 32 is supplied to location 1 within the RAM 31. Thus, the transfer will continue byte by byte until the full message has been written to memory locations falling within the range ZERO to SIZE-1.

The data buffer 23 allows the MCU and the DSP to communicate with each other efficiently. However, the level of storage within the data buffer is re-allocatable, such that optimum use is made of this storage space for whichever direction a transfer is taking place.

The present invention includes any novel feature or combination of features disclosed herein either explicitly or any generalisation thereof irrespective of whether or not it relates to the claimed invention or mitigates any or all of the problems addressed.

In view of the foregoing description it will be evident to a person skilled in the art that various modifications may be made within the scope of the invention.

Claims

1. A data buffer positionable between a first processing means and a second processing means, comprising storage means arranged to buffer data signals generated by each of said processing means for reception by the other of said processing means, and storage allocation means arranged to adjust the amount of storage provided by said storage means for transfers in each of said directions.
2. A data buffer according to claim 1, including a two-port random access memory, having one port for data transfer with said first processing means and a second port for data transfer with said second processing means.
3. A data buffer according to claim 1 or claim 2, including address generating means for generating addressing signals for the writing of data to said buffer or the reading of data from said buffer.
4. A data buffer according to claim 3, including address interpretation means, arranged to enable said address generating means in response to a particular addressing signal generated by said first processing or by said second processing means.
5. A data buffer according to claim 3 or claim 4, wherein said address generating means is arranged to generate addressing signals initiated from a predetermined value and to increment said signals so as to address a plurality of locations.
6. A data buffer according to claim 3 or claim 4, wherein said address signal generating means is arranged to generate addressing signals initiated from a predetermined value, including decoding means for selectively applying an offset to said addressing signals, depending upon whether a writing operation or a reading operation is being performed.
7. A data buffer according to any of claims 1 to 6, wherein said storage allocation means includes a register defining a location at which the transfer direction changes.
8. A processing system including a microcontroller and a digital signal processor, wherein a data buffer according to any of claims 1 to 7 is positioned between said microcontroller and said digital signal processor.
9. A signal processing system according to claim 8, wherein said microcontroller is interfaced to a keypad and a display of a mobile telephone and the

digital signal processor is interfaced to a microphone and a loudspeaker of said mobile telephone.

10. A method of buffering data being transferred between a first processing means and a second processing means, comprising steps of

storing data generated by either of said processing means;
reading said stored data by the other of said processing means; and
adjusting the amount of storage provided for transfers in each of said directions.

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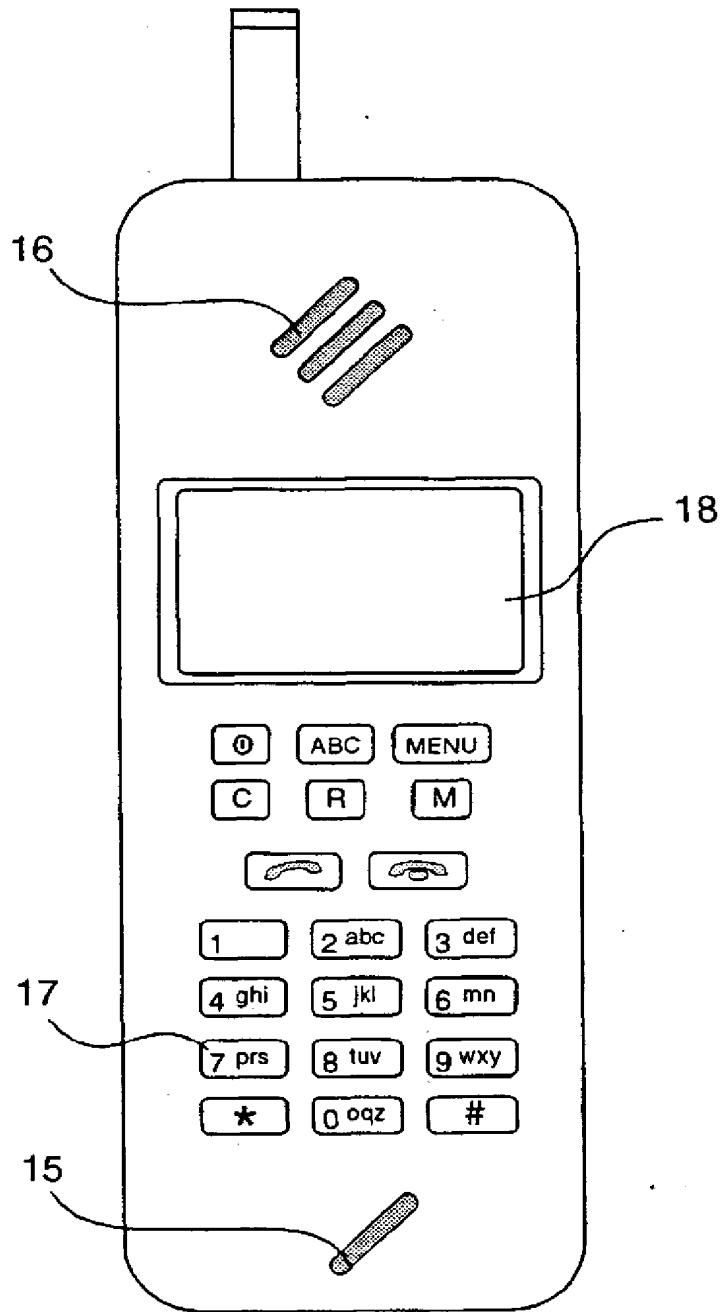


Figure 1

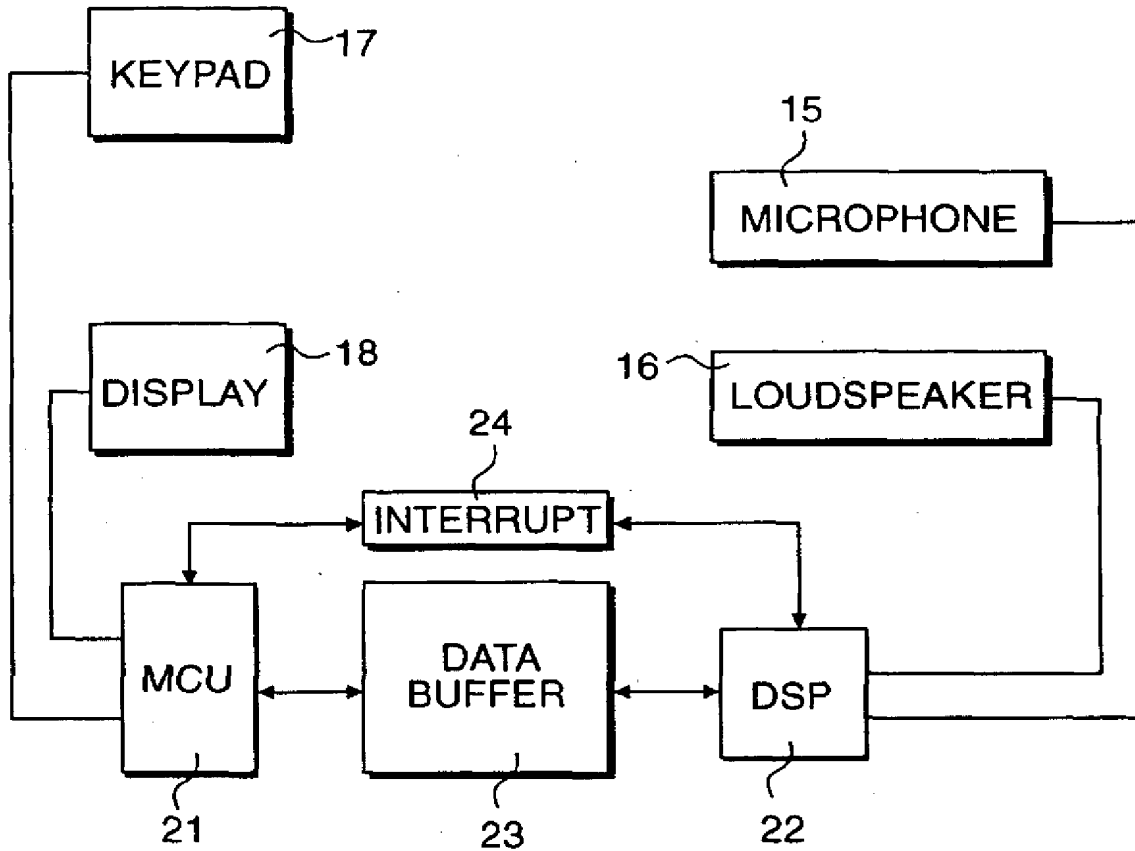


Figure 2

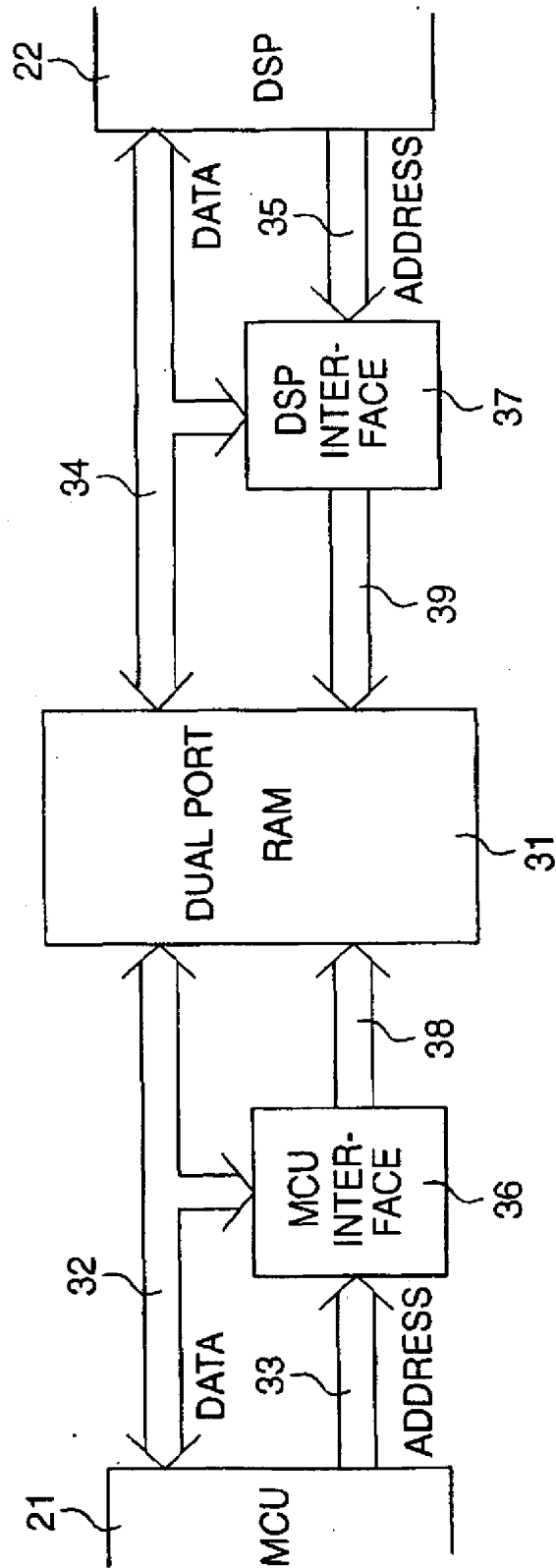


Figure 3

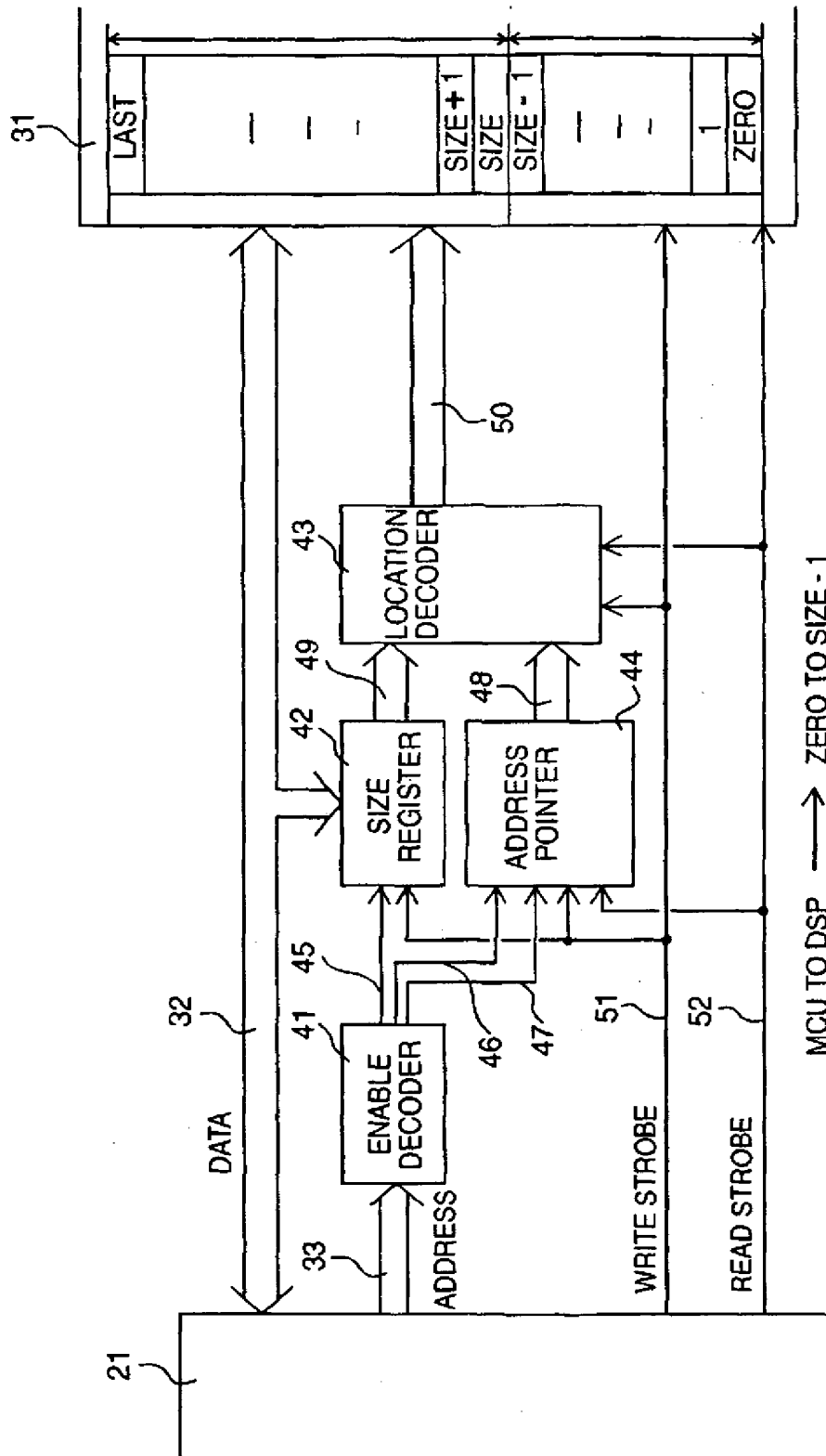


Figure 4



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Application Number
EP 96 30 0868

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Y	PATENT ABSTRACTS OF JAPAN vol. 010, no. 106 (P-449), 22 April 1986 & JP-A-60 237566 (OKI DENKI KOGYO KK), 26 November 1985, * abstract *	1,2,7,10	G06F15/16 G06F9/38
Y	--- PATENT ABSTRACTS OF JAPAN vol. 018, no. 110 (P-1698), 22 February 1994 & JP-A-05 303524 (NEC CORP;OTHERS: 01), 16 November 1993, * abstract *	1,2,7,10	
A	--- US-A-4 285 038 (SUZUKI SEIGO ET AL) 18 August 1981	3-6	
A	* column 2, line 19 - line 61; figure 1 *	6	
A	--- PATENT ABSTRACTS OF JAPAN vol. 015, no. 277 (E-1089), 15 July 1991 & JP-A-03 095916 (FUJITSU LTD), 22 April 1991, * abstract *	1,10	
A	--- PATENT ABSTRACTS OF JAPAN vol. 015, no. 251 (P-1220), 26 June 1991 & JP-A-03 081851 (SEIKO INSTR INC), 8 April 1991, * abstract *	1,2,9	
The present search report has been drawn up for all claims			
Place of search BERLIN		Date of completion of the search 6 June 1996	Examiner Deane, E
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

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